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(54) Transistor bridge circuit

(57) A bipolar transistor circuit to drive an associated load 14, such as a stepping motor, possibly by a high current flow thereto, comprises a bridge circuit, with the load to be connected between the mid-points of two pairs of series connected bipolar transistors T2, T3, and T4, T5. The bases of transistors T3 and T4 are respectively connected between the components of series combinations each of a bipolar transistor and a resistor T1, R1, and T6, R2, and the four series combinations are each connected between supply rails 10 and 11. The bases of transistors T1, T3, T5 and T6 are connected to an associated pulse source or sources 12, 13, 15 and 16 capable of driving ON and OFF the relevant transistors. With three different possible combinations of source outputs, current flows in either of the two directions within the transistor circuit and the load, or the load is isolated.

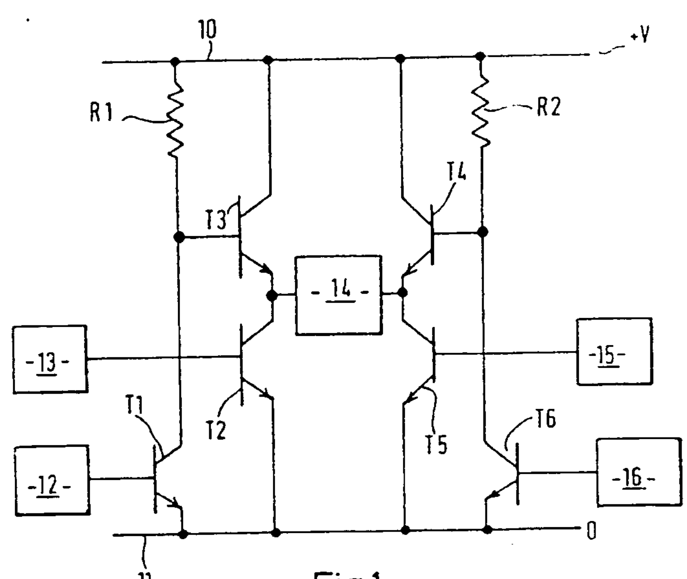

Fig.1

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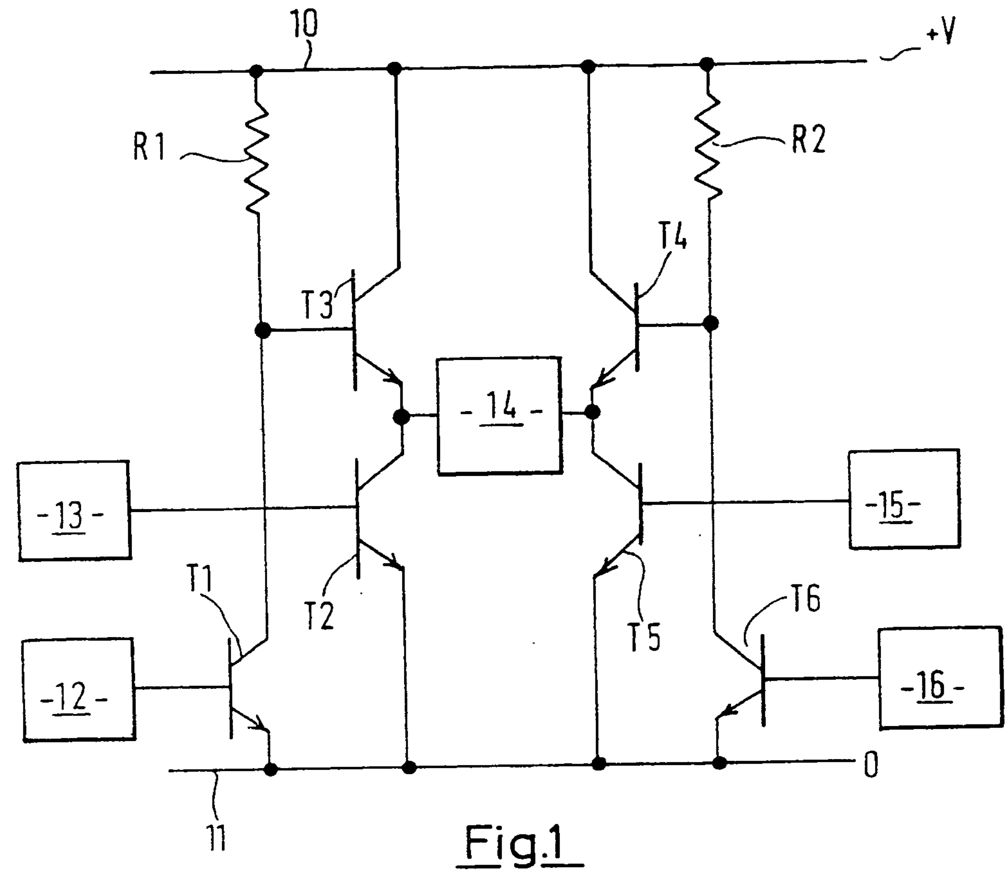

Fig.1

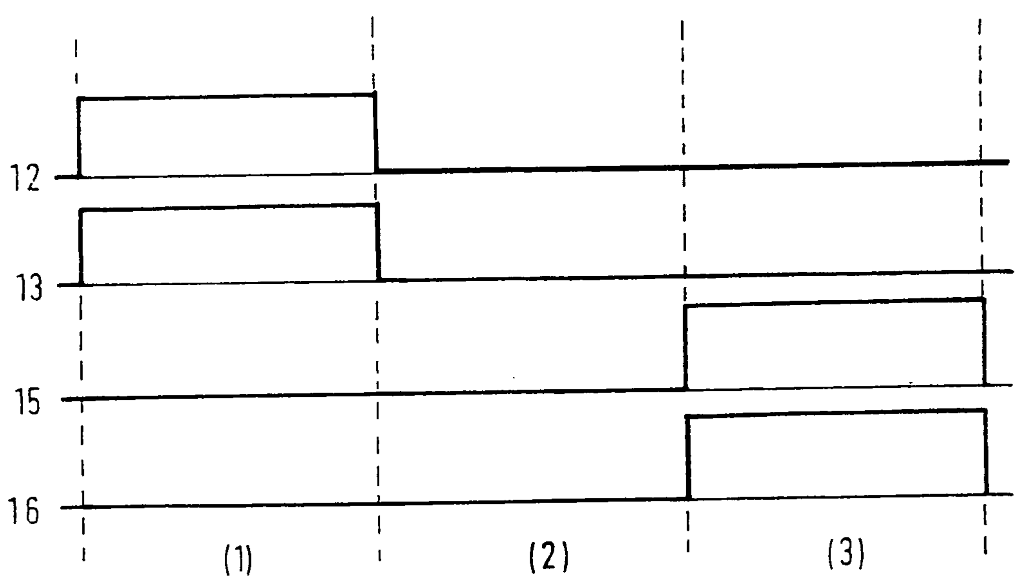

Fig.2

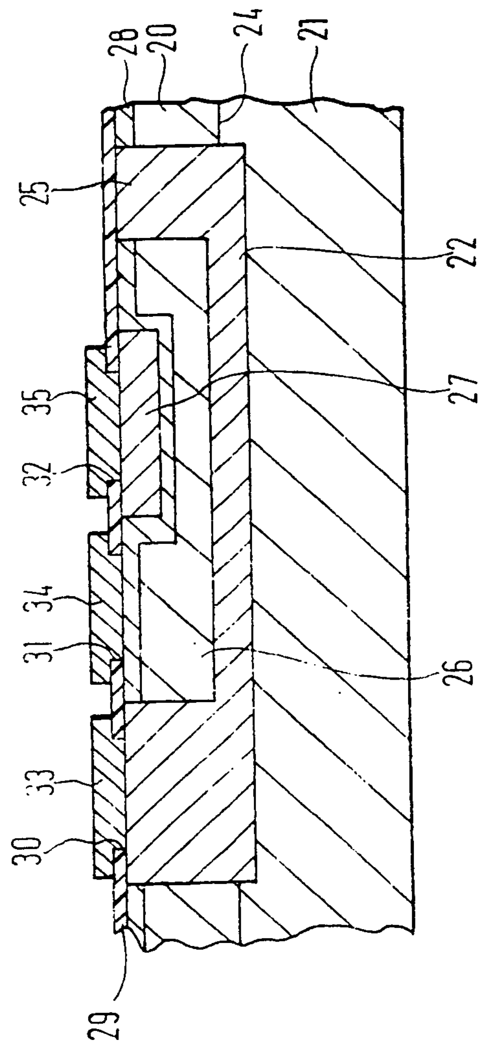

Fig.3

SPECIFICATION

Bipolar transistor circuits

This invention relates to bipolar transistor circuits, and in particular to bridge circuits each to drive an associated load in a bidirectional manner.

It is an object of the present invention to provide a bridge circuit to drive an associated load in a bidirectional manner, the arrangement being such that the associated load can be isolated by the bridge circuit.

According to the present invention a bipolar transistor circuit comprises a first transistor and a first resistor in series with each other, and in parallel with a series combination of second and third transistors, the first and second transistors being connected to a rail to be maintained at one reference potential level, and having their bases connected to associated pulse sources, the third transistor and the first transistor being connected to a rail to be maintained at another reference potential level, and the base of the third transistor is connected to a point between the first transistor and the first resistor, a point between the second and third transistors is connected to an associated load, the associated load is also connected to a point between fourth and fifth transistors, these transistors being in series with each other, and in parallel with a series combination of a second resistor and a sixth transistor, the fifth and sixth transistors being connected to the rail to be maintained at said one reference potential level, and having their bases connected to an associated pulse source or pulse sources, the fourth transistor and the second resistor being connected to the rail to be maintained at said other reference potential level, and the base of the fourth transistor is connected to a point between the second resistor and the sixth transistor, all the transistors of the circuit are of the same conductivity type, the associated pulse source or pulse sources are to cause to drive ON and OFF the transistors to which the pulse source or pulse sources are connected, the arrangement being such that current flows through the associated load and between the second and fourth transistors when the first and second transistors are driven ON, causing the third transistor to be driven OFF, and when the fifth and sixth transistors are driven OFF, current flows through the associated load and between the third and fifth transistors when the fifth and sixth transistors are driven ON, causing the fourth transistor to be driven OFF, and when the first and second transistors are driven OFF, and the associated load is isolated by the circuit when the first, second, fifth and sixth transistors are driven OFF.

Thus, the bipolar transistor circuit according to the present invention comprises a bridge circuit.

The bipolar transistors of the circuit each either comprises a single transistor, or each comprises a Darlington pair of transistors, functionally the equivalent of a single transistor. For convenience, where appropriate, in this specification, and the accompanying claims, the term transistor will be used to include a reference to a Darlington pair of transistors.

When the tranisistors are of NPN type, the current is to flow either from the fourth transistor to the second transistor, or from the third transistor to the fifth transistor, said one reference potential level is to be less positive than said other reference potential level, and the first, second, fifth and sixth transistors each is to be driven ON in response to a positive going part of a pulse, and is to be driven OFF in response to a less positive going part of a pulse.

According to another aspect the present invention comprises a combination of a bipolar transistor circuit of any one of the possible forms referred to above, and a pulse source or pulse sources associated with the transistor circuit, the associated pulse source or sources to control the different possible operations of the transistor circuit in the desired manner, the source or sources providing pulses to cause the transistor circuit to have the desired instantaneous operation, the different possible operations of the transistor circuit comprising causing the current to flow in either of the two possible directions within the transistor circuit and the associated load, and to isolate the associated load.

Separate pulse sources may be provided individually for each of the first, second, fifth and sixth bipolar transistors of the transistor circuit.

Alternatively, the arrangement may be such that two pulse sources control in unison corresponding pairs of bipolar transistors of the transistor circuit, the corresponding pairs comprising the first and second transistors, a pulse source being provided individually for each corresponding pair of transistors.

Alternatively, a common associated pulse source may be provided to control in unison all the bipolar transistors of the transistor circuit. The common pulse source may comprise common timing means, the bipolar transistor circuit performing a desired complete sequence of the different possible operations repetitively, the duration of the complete sequence of operations, and of each constituent operation of the complete sequence, being determined by the common timing means.

If a common pulse source, comprising timing means is not provided, the pulse source or the pulse sources associated with the bipolar transistor circuit may be arranged to be actuated to provide the desired pulses either under the control of an operator, or under the control of means associated with the pulse source or sources.

According to yet another aspect the present invention comprises a monolithic semiconductor device having embodied within a semiconductor body at least the bipolar transistor circuit of any one of the forms referred to above.

Each bipolar transistor of the semiconductor device may comprise an epitaxial base transistor, the semiconductor body of the device comprising a thin epitaxial layer of one conductivity type on a

substrate of the same conductivity type, the collector of the transistor including a heavily doped buried layer of the opposite conductivity type at a portion of the interface between the epitaxial layer and the substrate, the base at least including a portion of unmodified epitaxial material, and the emitter being provided at the surface of the epitaxial layer remote from the substrate. Thus, the bipolar transistor may have the so-called collector-diffusion-isolation construction, the collector also including a heavily doped portion of the opposite conductivity type extending through the epitaxial layer to contact the buried layer, the collector serving both to define the base within the epitaxial layer, and to isolate the transistor within the semiconductor body. Alternatively, the epitaxial-base bipolar transistor may have the so-called Isoplanar, or VIP, or V-ATE, construction. The use of epitaxial base transistors in the bridge circuit is advantageous in that such transistors conveniently can provide high current flows possibly required to drive the associated load, and are capable of being driven by advantageously small supply potentials. Further, they occupy only a small area of the surface of the epitaxial layer of the semiconductor body, and require only a few processing steps in their fabrication, compared with most other known transistor constructions. Hence, manufacturing yields are high.

There also may be embodied within the semiconductor device the load, and/or the pulse source or pulse sources associated with the bipolar transistor circuit.

The present invention will now be described by way of example with reference to the accompanying drawings, in which:—

Figure 1 is a diagram of a bipolar transistor circuit, comprising one embodiment according to the present invention, and to drive an associated load in a bidirectional manner, the associated load being isolated when the transistor circuit is in a quiescent state;

Figure 2 shows the pulse waveforms from associated pulse sources required to control the bipolar transistor circuit of Figure 1, the pulse waveforms being such that there is obtained a complete sequence of the different possible operations of the transistor circuit, and

Figure 3 is a section of a collector-diffusion-isolation bipolar transistor, comprising an epitaxial-base transistor suitable to be employed in the transistor circuit of Figure 1.

The bipolar transistor circuit illustrated in Figure 1 comprises a bridge circuit with an NPN transistor T1 in series with a resistor R1, and the resistor R1 is connected to a supply rail 10 maintained at a reference potential level of +V. The transistor T1 is connected to a return rail 11 maintained at zero potential. The base of the transistor T1 is connected to an associated pulse source, indicated generally at 12. Parallel to the resistor R1 and the transistor T1 are two NPN transistors T2 and T3 in series with each other, the transistor T2 being connected to the return rail 11, and the transistor T3 being connected to the supply rail 10. The base of the transistor T2 is connected to an associated pulse source indicated generally at 13. The base of the transistor T3 is connected to a point between the transistor T1 and the resistor R1. A point between the transistors T2 and T3 is connected to a load 14 associated with, but not comprising part of, the bridge circuit, the load to be driven in a bidirectional manner. The associated load 14 is also connected to a point between two NPN transistors T4 and T5 connected in series with each other, the transistor T4 being connected to the supply rail 10, and the transistor T5 being connected to the return rail 11. The base of the transistor T4 is connected to a point between a resistor R2 and an NPN transistor T6, the resistor R2 being connected to the supply rail 10, and the transistor T6 being connected to the return rail 11. The base of the transistor T5 is connected to an associated pulse source indicated generally at 15. The base of the transistor T6 is connected to an associated pulse source indicated generally at 16.

The pulse sources 12, 13, 15 and 16, which are not considered to be part of the bridge circuit, are arranged to control their associated transistors, respectively, T1, T2, T5 and T6, so that these transistors are driven ON or OFF.

The states of the transistors T3 and T4 each are determined by the states of the other transistors of the bridge circuit.

In operation, current flows through the associated load 14, either via the transistors T3 and T5, or via the transistors T4 and T2, and it is possible to isolate the associated load by driving OFF the transistors T1, T2, T5 and T6.

The pulse waveforms from the associated sources 12, 13, 15 and 16 to control the bridge circuit for a complete sequence of three different possible operations of the bridge circuit are shown at (1), (2) and (3) in Figure 2, each associated source providing one pulse in the complete sequence of the different possible operations.

In this complete sequence of the different possible operations of the bridge circuit, as indicated at (1), initially current is flowing through the transistors T4 and T2 via the associated load 14. The transistor T2 is driven ON in response to the positive going part of the pulse from the associated source 13, and this causes the transistor T3 to be driven OFF. The transistors T5 and T6 are driven OFF in response to the less positive going parts of the pulses from their associated sources 15 and 16. As indicated at (2), to isolate the associated load 14, the transistors T1 and T2 are then also driven OFF in response to the less positive going parts of the pulses from their associated sources 12 and 13. The bridge circuit then can be considered to be in a quiescent state. As indicated at (3), to cause the current to flow through the transistors T3 and T5, via the associated load 14, the transistor T5 is driven On in response to the positive going part of the pulse from its associated source 15. Transistor T6 is driven ON in response to the positive going part of

the pulse from its associated source 16, and this causes the transistor T4 to be driven OFF. The order of this sequence of operations may be reversed.

Because the associated load 14 is isolated when the bridge circuit is in its quiescent state, the current flow through the bridge circuit is small when it is in its quiescent state. Thus, the ratio of the current flow through the bridge circuit when current is flowing in either of the two possible directions through the associated load, to the current flow through the bridge circuit when the bridge circuit is in its quiescent state, is large. Hence, the associated load may comprise a stepping motor in a watch, or a clock, or a servo system, or a positioning system. Because the associated load is isolated when the bridge circuit is in its quiescent state the associated load also may comprise an electrolytic or electrochromic display.

Further, the bridge circuit requires only an advantageously small potential +V on the supply rail 10, and so the bridge circuit conveniently may be driven by a small electrolytic cell.

For one embodiment of a bridge circuit according to the present invention a current of up to 0.5 milliampere can flow in either direction through the associated load, whereas when the bridge circuit is in a quiescent state the current flow through the bridge circuit is at most 0.5 microampere. The potential of the supply rail is 2.4 volts, and the resistors R1 and R2 are each 400 Kilo-ohms.

If the bipolar transistors are replaced by Darlington pairs it is required that the potential of the supply rail is 4.5 volts and the resistors R1 and R2 are each 2.2 Megohms. A current of up to 100 milliamperes can flow in either direction through the associated load, whereas when the bridge circuit is in a quiescent state the current flow through the bridge circuit is at most 0.5 microampere.

The associated pulse sources 12, 13, 15 and 16 may have any convenient construction.

Alternatively, a sole, common associated pulse source may be provided, possibly by providing common timing means, the complete sequence of the three different possible operations of the bridge circuit being obtained repetitively, the duration of the complete sequence of operations, and of each constituent operation of the complete sequence, being determined by the common timing means.

Alternatively, the pulse sources 12 and 13, and the pulse sources 15 and 16, may be combined.

The associated pulse source or pulse sources may be actuated, to provide the desired pulses either under the control of means associated with the pulse source or sources, such as the character generator of an electrolytic or electrochromic display system, or under the control of an operator. Hence, there may be obtained an incomplete sequence of the different possible operations, and the different possible operations may not be obtained in a repetitive manner.

It is advantageous that the bipolar transistor circuit is embodied within the semiconductor body of a monolithic semiconductor device.

Each transistor of such a semiconductor device may comprise an epitaxial base transistor, because such transistors conveniently can provide the high current flows possibly required to drive the associated load, and are capable of being driven by advantageously small supply potentials.

One such epitaxial base transistor comprises a transistor with the so-called collector-diffusion-isolation construction, and is shown in Figure 3. Thus, the silicon semiconductor body of the monolithic device comprises a thin P-type epitaxial layer 20 on a P-type substrate 21. During the formation of the semiconductor body a heavily doped buried layer 22 of N+ conductivity type is provided at a portion of the interface 24 between the epitaxial layer 20 and the substrate 21. The collector of the transistor comprises both the N+ type buried layer 22 and an N+ type isolation barrier 25 for the transistor, the isolation barrier 25 being provided so as to extend through the epitaxial layer 20 into contact with the buried N+ type layer 22. The collector 22, 25 defines a P-type region 26 including unmodified epitaxial material, and subsequently an N+ type emitter 27 is formed in the base 26. The collector also serves to isolate the transistor within the semiconductor body.

A collector-diffusion-isolation transistor may be provided with a heavily doped P+ type surface portion 28 for the epitaxial layer, this P+ type surface portion being provided in a non-selective diffusion step before the formation of the emitter. Thus, the emitter is surrounded within the semiconductor body by a P+ type region. This causes the gain-bandwidth product of the transistor to be increased, and helps to prevent the inversion of surface portions of the epitaxial layer.

The illustrated transistor is formed by a known method, and during the final diffusion process steps a passivating layer 29 of silicon oxide is provided on the otherwise exposed surface of the epitaxial layer 20. Apertures 30, 31 and 32 are formed in the passivating layer 29, respectively, to expose portions of the collector 22, 25, and base 26 and the emitter 27. Contacts 33, 34 and 35 are provided, respectively within the apertures 30, 31 and 32 the contacts being provided from an initially-continuous metal layer deposited on the passivating layer and within the apertures.

The other types of circuit element (not shown), are included within the monolithic device, such as the resistors R1 and R2 of the bridge circuit according to the present invention, each have a construction closely resembling that of the collector-diffusion-isolation transistor described above. The provision of the P+ type surface portion 28 in a non-selective diffusion step, as referred to above, serves to help to define accurately the resistors required within the semiconductor body.

Alternatively, the transistor having the epitaxial-base construction may have the so-called

Isoplanar construction, or VIP construction, or V-ATE construction, all not shown. Each such construction has the base including an unmodified portion of an epitaxial layer of one conductivity type, the epitaxial layer being on a substrate of the same conductivity type, the base being contiguous with a buried layer of the opposite conductivity type, and the buried layer partially comprising the collector. Each such transistor construction closely resembles that of a collector-diffusion-isolation transistor described above except that the isolation barrier does not comprise part of the collector. Instead the collector, in addition to including the buried layer, includes a region of the epitaxial layer modified by inclusion of an impurity characteristic of the opposite conductivity type, and extending to the surface of the epitaxial layer remote from the substrate. An isolation barrier of insulating material is provided. In an Isoplanar transistor the isolation barrier is substantially the same shape as that of a collector-diffusion-isolation transistor, but the isolation barrier is wholly of silicon oxide; in a V-ATE transistor the isolation barrier is a 'V'-section groove etched through the epitaxial layer and coated with silicon oxide; and in a VIP transistor the isolation barrier is a 'V'-section groove etched through the epitaxial layer, coated with silicon oxide, and filled with polycrystalline silicon material.

Collector-diffusion-isolation transistors, and epitaxial-base transistors in general, occupy only a small area of the surface of the epitaxial layer of the silicon semiconductor body, and require only a few processing steps in their fabrication, compared with most other known transistor constructions. Hence, manufacturing yields are high.

A monolithic semiconductor device according to the present invention, and embodying a bipolar transistor circuit according to the present invention, also may embody other circuits than the transistor circuit. For convenience, and if possible, the monolithic device may also embody the pulse source or sources, and/or the load, associated with the bridge circuit.

The transistors of the bridge circuit all may be of PNP type, rather than being of NPN type, and the current flows either from the transistor T2 to the transistor T4, or from the transistor T5 to the transistor T3. The supply rail is connected to the transistors T1, T2, T5 and T6, and the return rail is connected to the transistors T3 and T4, and to the resistors R1 and R2. The potential of the supply rail is more negative than the potential of the return rail. The transistors T1, T2, T5 and T6 each are driven ON in response to a negative going part of a pulse, and are driven OFF in response to a less negative going part of a pulse.

CLAIMS

1. A bipolar transistor circuit comprising a first transistor and a first resistor in series with each other, and in parallel with a series combination of second and third transistors, the first and second transistors being connected to a rail to be maintained at one reference potential level, and having their bases connected to associated pulse sources, the third transistor and the first resistor being connected to a rail to be maintained at another reference potential level, and the base of the third transistor is connected to a point between the first transistor and the first resistor, a point between the second and third transistors is connected to an associated load, the associated load is also connected to a point between fourth and fifth transistors, these transistors being in series with each other, and in parallel with a series combination of a second resistor and a sixth transistor, the fifth and sixth transistors being connected to the rail to be maintained at said one reference potential level, and having their bases connected to an associated pulse source or pulse sources, the fourth transistor and the second resistor being connected to the rail to be maintained at said other reference potential level, and the base of the fourth transistor is connected to a point between the second resistor and the sixth transistor, all the transistors of the circuit are of the same conductivity type, the associated pulse source or pulse sources are to cause to drive ON or OFF the transistors to which the pulse source or pulse sources are connected, the arrangement being such that current flows through the associated load and between the second and fourth transistors when the first and second transistors are driven ON, causing the third transistor to be driven OFF, and when the fifth and sixth transistors are driven OFF, current flows through the associated load and between the third and fifth transistors when the fifth and sixth transistors are driven ON, causing the fourth transistor to be driven OFF, and when the first and second transistors are driven OFF, and the associated load is isolated by the circuit when the first, second, fifth and sixth transistors are driven OFF.

2. A transistor circuit is claimed in claim 1 in which a current of up to 0.5 milliampere can flow in either direction through the associated load.

3. A transistor circuit as claimed in claim 1 or claim 2 in which each of the constituent bipolar transistors comprises a Darlington pair of transistors, functionally the equivalent of a single transistor.

4. A transistor circuit as claimed in claim 3 in which a current of up to 100 milliamperes can flow in either direction through the associated load.

5. A transistor circuit as claimed in any one of the preceding claims in which the transistors are of NPN type, the current is to flow either from the fourth transistor to the second transistor, or from the third transistor to the fifth transistor, said one reference potential level is to be less positive than said other reference potential level, and the first, second, fifth and sixth transistors each is to be driven ON in response to a positive going part of a pulse, and is to be driven OFF in response to a less positive going part of a pulse.

6. A combination of a bipolar transistor circuit

as claimed in any one of claims 1 to 5, and a pulse source or pulse sources associated with the transistor circuit, the associated pulse source or sources to control the different possible operations of the transistor circuit in the desired manner, the source or sources providing pulses to cause the transistor circuit to have the desired instantaneous operation, the different possible operations of the transistor circuit comprising causing the current to flow in either of the two possible directions within the transistor circuit and the associated load, and to isolate the associated load.

7. A combination as claimed in claim 6 in which separate pulse sources are provided individually for each of the first, second, fifth and sixth transistors of transistor circuit.

8. A combination as claimed in claim 6 in which two pulse sources are arranged to control in unison corresponding pairs of bipolar transistors of the transistor circuit, the corresponding pairs comprising the first and second transistors, and the fifth and sixth transistors, a pulse source being provided individually for each corresponding pair of transistors.

9. A combination as claimed in claim 6 in which a common pulse source is provided to control in unison all the bipolar transistors of the transistor circuit.

10. A combination as claimed in claim 9 in which the common pulse source comprises common timing means, the bipolar transistor circuit performing a desired complete sequence of the different possible operations repetitively, the duration of the complete sequence of operations, and of each constituent operation of the complete sequence, being determined by the common timing means.

11. A combination as claimed in any one of claims 7 to 9 in which the pulse source or the pulse sources associated with the bipolar transistor circuit are arranged to be actuated to provide the desired pulses under the control of an operator.

12. A combination as claimed in any one of claims 7 to 9 in which the pulse source or the pulse sources associated with the transistor circuit are arranged to be actuated to provide the desired pulses under the control of means associated with the pulse source or sources.

13. A semiconductor device having embodied within a semiconductor body at least the bipolar transistor circuit as claimed in any one of claims 1 to 5.

14. A device as claimed in claim 13 in which each bipolar transistor comprises an epitaxial base transistor, the semiconductor body comprising a thin epitaxial layer of one conductivity type on a substrate of the same conductivity type, the collector of the transistor including a heavily doped buried layer of the opposite conductivity type at a portion of the interface between the epitaxial layer and the substrate, the base at least including a portion of unmodified epitaxial material, and the emitter being provided at the surface of the epitaxial layer remote from the substrate.

15. A device as claimed in claim 14 in which the bipolar transistor has the so-called collector-diffusion-isolation construction, the collector also including a heavily doped portion of the opposite conductivity type extending through the epitaxial layer to contact the buried layer, the collector serving both to define the base within the epitaxial layer, and to isolate the transistor within the semiconductor body.

16. A device as claimed in claim 14 in which the epitaxial-base bipolar transistor has the so-called Isoplanar, or VIP, or V-ATE construction.

17. A device as claimed in any one of claims 13 to 16 in which there is also embodied the load associated with the bipolar transistor circuit.

18. A device as claimed in any one of claims 13 to 17 in which there is embodied the combination of the bipolar transistor circuit and a pulse source or pulse sources associated with the bipolar transistor circuit, and as claimed in any one of claims 6 to 12.

19. A bipolar transistor circuit substantially as described herein with reference to Figures 1 and 2 of the accompanying drawings.

20 A combination of a bipolar transistor circuit and associated pulse sources substantially as described herein with reference to Figures 1 and 2 of the accompanying drawings.

21. A semiconductor device substantially as described herein with reference to the accompanying drawings.

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